AUTOMATED I/O LIBRARY GENERATION FOR INTERPOSER BASED SYSTEM-IN-PACKAGE INTEGRATION OF MULTIPLE HETEROGENEOUS DIES

A Dissertation
Presented to
The Academic Faculty

By

Minah Lee

In Partial Fulfillment
of the Requirements for the Degree
Masters of Science in
School of Electrical and Computer Engineering

Georgia Institute of Technology

December 2019

AUTOMATED I/O LIBRARY GENERATION FOR INTERPOSER BASED SYSTEM-IN-PACKAGE INTEGRATION OF MULTIPLE HETEROGENEOUS DIES

Approved by:

Dr. Saibal Mukhopadhyay, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Madhavan Swaminathan
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Sung Kyu Lim
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: December 6, 2019

To my parents

ACKNOWLEDGEMENTS

First, I would like to thank my advisor, Prof. Saibal Mukhopadhyay, for his constant advice and support he has provided throughout this research. His invaluable research vision has deeply inspired me and his considerate guidance has allowed me to take pleasure in all the moments during the research. I would also like to thank my thesis committee members, Prof. Madhavan Swaminathan and Prof. Sung Kyu Lim for their invaluable comments during this research.

I am grateful to former and current GREEN Lab members, especially Dr. Arvind Singh for his kind guidance and help. I would also like to thank Hakki M.Torun and Jinwoo Kim, who have contributed to this research.

I would like to thank my undergraduate advisor, Prof. Jae-Joon Kim, who has provided my first passion for research and allowed the decision to graduate studies and research.

I give my greatest thank to my parents for their endless love and care all the time. Their continuous supports always allowed me confident and passionate in my life.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

System-in-Package (SiP) integration of multiple dies in a single package can achieve much higher performance than on-board integration of ICs while reducing the design cost / effort compared to large System-on-Chips (SoCs). However, a major challenge in design of SiPs with many dies is automated design and insertion of Input/Output (I/O) cells to minimize energy and delay of the wire traces. The research presents an automated cell library generation flow for all-digital I/O circuits for SiP integration. Given parameterized models of SiP wire traces, our method automatically designs, optimizes, and generates layouts of I/O cells for delay/energy minimization. The proposed flow is demonstrated on interposer based SiP integration considering 28nm CMOS technology and 65nm BEOL technology. Given a multi-die SiP design and associated interposer wire-traces, the research demonstrates that automated I/O library cell generation can reduce maximum die-to-die communication delay or energy. The research demonstrate the proposed flow for various interposer parameters and SiP designs to show the feasibility of chip-interposer co-design.

CHAPTER 1
INTRODUCTION

System-on-Chip (SoC) integration of diverse functional units have been the driver of electronic and computing systems. However, the complexity and cost of designing a complex SoC in advanced CMOS nodes have increased significantly over the last decade [1]. Consequently, alternative packaging technologies such as interposers (2.5D), 3-Dimensional (3D) integrated circuits (ICs), multi-chip-modules (MCMs) have received major attentions to integrate diverse functions [2, 3, 4]. The system-in-package (SiP) allows integration of digital logic, memory, analog, mixed-signal, and RF functions, which are potentially designed in heterogeneous technologies, in a single module [5, 6, 7, 8, 9]. Recent breakthroughs in silicon interposer based 2.5D integration technologies [7, 8, 9] demonstrate scalable systems with comparable performance to SoC solutions and ease of integration like conventional packaging. The ability to re-use intellectual property (IP) as individual dies in a SiP promises amortization of design effort/cost over a longer lifecycle of IPs [10]. Overall, SiP promises SoC-like performances but can reduce design cost and complexity and increase yields [5, 6, 7, 8, 9]. However, lack of design tools remains a critical challenge for large-scale commercial adoption of 2.5D based SiP integrations [10]. This paper develops an automation approach to address the I/O design tool challenge associated with die-to-die on-interposer signaling for given multi-die SiP design and associated interposer wire-traces.

In a SoC, different IPs communicate through on-chip wires (Figure. 1.1(a)). The on-chip wires in advanced CMOS processes, which are highly diffusive in nature, can be modeled as distributed RC network[11]. CMOS inverters/buffers based transmitter/receiver can drive on-chip wires. Design automation tools exist to characterize on-chip wires, optimize their drivers/receivers, and perform buffer insertion to recover signal slew and minimize

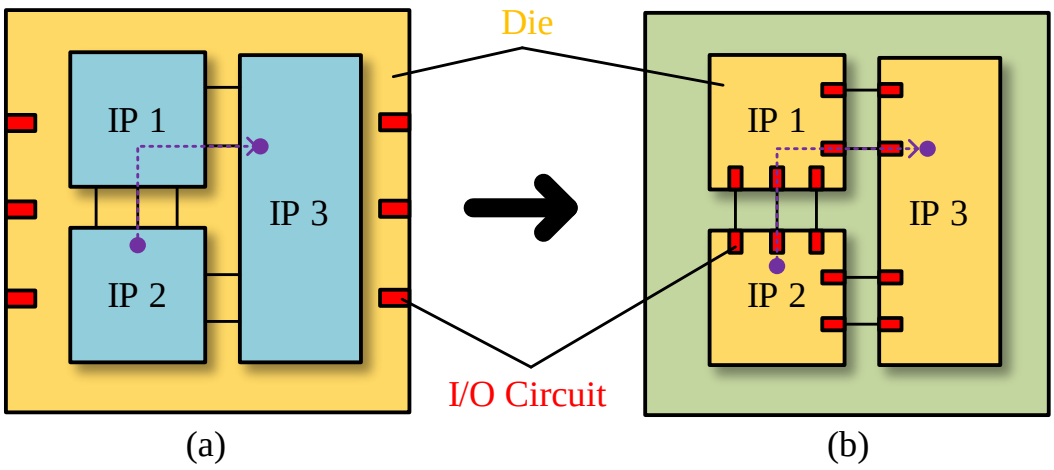

Figure 1.1: (a) On-chip wires without any need for I/O circuits for SoC integration, (b) I/O circuits are required for SiP integration to drive long interposer wires.

wire delay/energy. However, when the same SoC is partitioned into multiple dies and integrated as a SiP, the on-chip wires between IPs are replaced by die-to-die (D2D) interconnects in the interposer (Fig. 1.1(b)). To minimize performance (or energy) loss, signaling through on-interposer wires must be optimized for minimum communication delay or energy, similar to the case for on-chip wires. Unlike on-chip wires where delay/energy minimization is performed by optimal insertion/placement of inverters/buffers, in the case of on-interposer wires the minimization must be performed by optimally designing the I/O cells. In addition, wires in silicon interposers have larger linewidth and show inductive properties. Hence, the transceiver circuits which minimize delay/energy of die-to-die signal while ensuring good signal quality must be designed taking transmission line behavior of on-interposer wires into considerations [12].

Moreover, traditional I/O cells for off-chip signaling are usually designed to match target impedance. As there are many on-interposer wires with varying impedance characteristics in SiP, it is critical to develop an automated approach for optimal design of I/O cells for on-interposer signaling. Such optimization needs to go beyond matching a target impedance, and explicitly consider delay and/or energy as cost function. In addition, the traditional I/O cells are complex mixed-signal circuits, consume appreciable power, and

require custom design. The total number of I/O cells connecting on-interposer wires in a SiP will be much larger than number of off-chip I/Os in the original SoC (Fig. 1.1). Hence, directly adopting complex I/O cells for off-chip signaling in SoC to die-to-die signaling in SiP will reduce power-efficiency and increase design effort. I/O cells (drivers/receivers) for SiP should be simple and provide optimal delay/energy.

The design of drivers/receivers for SiP needs to be automatically generated to provide optimal design for on-interposer wires with low design complexity and cost. On one hand, driver/receiver circuits for on-interposer wires should function similar to I/O circuits for off-die communication in traditional SoCs to maintain high signal quality through inductive wires. For example, similar to I/O cells for traditional packaging, the I/O cells for dies in SiP should be designed to cope with coupled, frequency dependent RLGC properties of on-interposer wires, instead of only RC properties in on-chip wires. On the other hand, driver/receiver circuits for on-interposer wires should be small and simple enough similar to I/O circuits for on-chip communications to automatically generate for large SiP design and reduce design cost. All-digital I/O cells with full-swing signaling, similar to on-chip wires, are desirable to achieve this goal.

The research presents *an automated library generation flow of all-digital I/O cells for given 2.5D (interposer) technology and varying trace lengths*. Figure. 1.2 shows the overview of the proposed cell library which considers package specification and design goals, and generates I/O cell with layout and its timing/power library. The proposed tool can be applied to both system-in-package and system-in-interposer as long as one is using an all-digital, full-swing (single-ended or differential), and moderate frequency (1-5 GHz) signaling. Such signaling is feasible mostly in low-to-moderate (1mm-10mm) distance interconnects in system-in-package and system-on-interposer integrations. However, to demonstrate the tool flow, this research mostly focus on system-on-interposer systems for wire-modeling. The research first present a chip-interposer co-simulation environment that couples SPICE models for I/O cells (drivers, receivers) with parametric models of in-

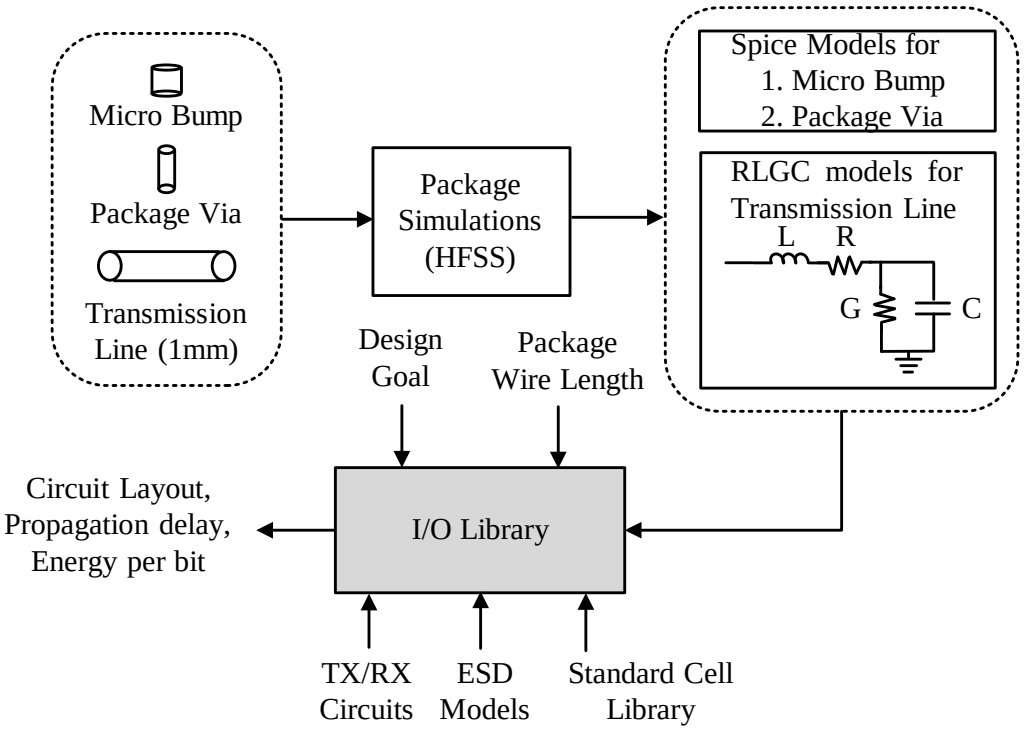

Figure 1.2: Overview of proposed I/O cell library generation.

terposer wire traces. The co-simulation characterizes delay and energy of the physical link (driver, wire trace, and receiver), which is designed with full-swing digital signaling and digital CMOS inverters, similar to on-chip communication. Using co-simulation, a design flow is developed that automatically generates all-digital I/O cell library. The tool generates driver/receiver that gives minimum delay/energy (design goal, i.e. electrical cost function) for given interposer technology and wire length (design specification) with 90% voltage swing constraints at the input of receiver (optimization constraints). The proposed flow allows a designer to define a cost function which includes delay, energy, target impedance, or area of I/O cells, etc. To demonstrate the flow, a cost function is defined as delay and energy minimization through this research.

Proposed tool generates cell library both as soft-macro (register transfer logic, RTL level) and hard macro (layout) in a target CMOS technology. The soft macro can be integrated with the RTL description of the IP facilitating early-stage design space exploration

of SiP; while the hard macro can be integrated with the layout of an IP facilitating physical design of the multi-die SiP. Auto-generation of I/O cells is demonstrated for various design goals (minimum delay/energy), different interposer parameters, different wire-length, and ESD protections. With a case study on a SiP-based multi-core mesh NOC structure, this research shows that wire distribution dependent optimization of I/O library cell can help enhance delay/energy characteristics of die-to-die communication in SiP, compared to design of fixed I/O cells for target output impedance. For various case studies such as SiP design with non-neighboring connection or heterogeneous signaling, I/O design methodology is presented using the proposed generation flow to meet the design goal.

The rest of the thesis is organized as follows: In Chapter 2, the detailed background and literature survey is presented. Chapter 3 presents the co-simulation flow of chip and interposer. Chapter 4 presents automated I/O cell library generation flow. Chapter 5 shows some experimental results of interposer model/wire length dependent I/O library generation and applications on various SiP designs. Chapter 6 describes the key research contributions and provides future research direction.

CHAPTER 2

BACKGROUND

2.1 I/O Circuits for On-Chip Wire

In past few decades, researchers have explored different signaling schemes to drive long on-chip wires at high data rates and low energy [12]. However, most of these work have only looked at RC characteristics of on-chip wires; employing current mode [13] or low voltage differential signaling [14], or utilizing complex capacitor based pre-emphasis and equalization circuits [15],[16] as well expensive calibration techniques to improve timing/voltage margins [17]. Additionally, these high data rate signaling techniques implement source-synchronous links to remove any mismatch between clock and data lines resulting from variations in operating conditions or crosstalk [18]. Most of these schemes are not designed to consider inductive characteristic of interposer wires. Moreover, the designs lead to custom cells, and are difficult to integrate in a RTL-level tool.

2.2 Various Off-Chip Signaling

Recently, some researchers have explored silicon/glass based 2.5D package technologies [19],[20], signaling schemes for the D2D interconnects for high data rates at low energy [21],[22]. Sawyer et al. [19] demonstrate redistribution layers (RDL) on the surface of glass for very high speed (28Gbps) signaling while Sundaram et al. demonstrate feasibility of low-cost and low-loss 3D silicon interposer without TSVs for high bandwidth logic-to-memory interconnects [20]. Lee et al. [21] present an energy-efficient current mode signaling scheme for glass based interposer wire for up to 3Gbps of data rate. It utilizes open-drain transmitter with 1-tap pre-emphasis and a current sense amplifier as receiver. Even though this scheme achieves very good energy efficiency, the driver and

receiver circuits are not friendly to digital synthesis, place and route flows and glass interposer technologies are not easily integrable with silicon based CMOS processes. W. S. Liao et al [22] present a heterogeneous system consisting of a RF receiver, baseband processor and DRAM, all in different technologies integrated in 3D on CoWoS. However, the focus of their work is on electrical characterization with a very fast built-in-self-test (BIST) algorithm targeted for heterogeneous integration. Similarly, M. S. Lin et al. [23] present a eDRAM PHY operating at very low voltage swing (0.3V) on 2.5D CoWoS. More recently, S. Dinakarrao [24] propose Q-learning based self-adaptive output-voltage swing adjustment and further present a 2.5D integrated multicore network-on chip, which consists of microprocessor die, memory die, and accelerator die with 2.5D silicon interposer I/Os. Y. Jeon et al. [25] propose an on-silicon-interposer passive equalizer for next generation High Bandwidth Memory (HBM). However, most of these schemes adopt I/Os in analog mixed-signal circuits, which consume large amount of energy. Also they require custom design that leads to high design cost, especially for large heterogeneous SiP system.

CHAPTER 3

CHIP-INTERPOSER CO-SIMULATION

A chip-interposer co-simulation flow is developed to accurately characterize delay and energy in the physical link (driver, wire, and receiver) of an interposer wire. The transceiver circuits and signaling mimics driving on-chip wires.

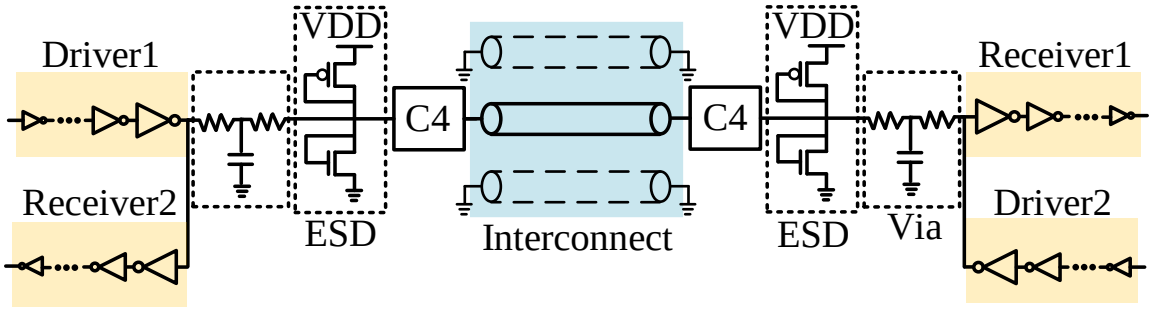

Figure 3.1: All-digital I/O and full-swing digital signaling.

The proposed design uses full-swing digital signaling and all-digital I/Os based on CMOS inverters as transceivers as shown in the Figure. 3.1. All-digital I/O requires full swing signaling at the receiver interface, eliminating receiver side termination, which helps in minimizing the total power. However, compared to on-chip wires, interposer wires in SiP have significant inductance, specifically for longer wires, and show transmission line behavior even at moderate frequencies ($\sim$1-2 GHz). Therefore, accurate interconnect model that includes all the full-wave EM effect of interconnects is necessary for co-simulation.

As mentioned earlier, interconnects in the interposer show a strong inductive behavior that cannot be ignored in the SPICE model. In order to capture the impedance and coupling profiles of these interconnects accurately, a full-wave EM solver needs to be utilized. However, such solvers tend to be CPU extensive especially for multi-scale structures seen in chip-to-chip traces on the interposer.

To overcome this CPU extensive process and efficiently automate the SPICE model generation process without losing accuracy, machine learning (ML) techniques are used. First, a moderate amount of training data from a full-wave EM solver, Ansys HFSS, is collected using single-frequency simulations by storing the full RLGC matrices of the interconnects. Note that the interconnect thicknesses on the interposer have the same order of magnitude with the skin depth at desired frequency of operation. Hence, the transition of self and mutual R and L from DC to higher frequencies constitute the majority of the frequency dependent behavior. Since the proposed technique utilizes full-wave EM simulations to extract the RLGC parameters that accounts for the complete skin, proximity and edge effects, this behavior is accurately captured in the final model.

As training data is collected only by using single-frequency simulations as opposed to high-bandwidth frequency sweep ranging from DC to high GHz regime, the training data collection time is significantly reduced. Then, an Additive Gaussian Process (ADD-GP)[26] is trained that takes geometric parameters of the interconnects and a range of frequency as input and outputs the frequency dependent RLGC matrices. This is then converted into S-Parameters, which is then used by broadband spice generator of Keysight ADS to generate the final SPICE model. The same steps are repeated for modeling C4 bumps, but the ADD-GP model is trained to directly predict S-Parameters for this case. The framework is summarized in Figure. 3.2 and detail description can be found in [27]. The ADD-GP model shows $\sim$97% accuracy and requires only 2 seconds to generate the broadband spice model as opposed to 2 hours required by full-wave EM solver. The total training time required to derive the model is only 5 hours since there is no high-bandwidth frequency sweeps involved in this step.

Final hspice compatible models are coupled with circuit level models of the driver/ receiver in hspice. Hence, the whole physical link can be simulated in hspice and obtain propagation delay and energy. As the proposed I/O generation tool considers full-wave EM effect of interconnects, generated I/O design considers not just loss/cross-talk, but

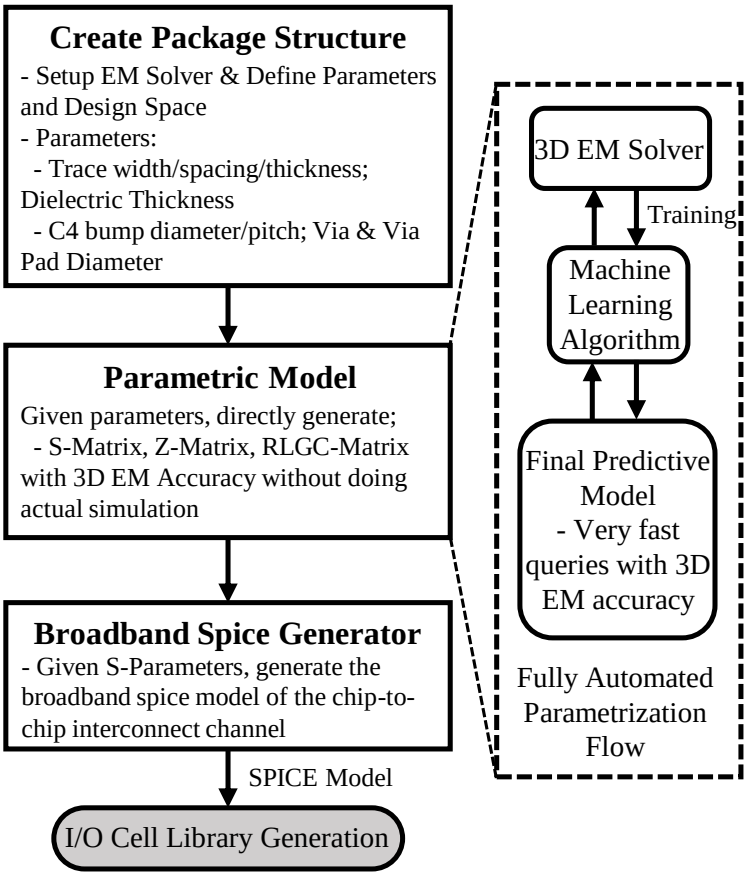

Figure 3.2: Package model generation [28].

skin/proximity effect and non-uniform current distribution along the width of the interconnects along with all higher modes of propagation that occur in discontinuities such as bump-to-via transition.

CHAPTER 4

CELL LIBRARY GENERATION FLOW

For a given interposer model and wire length, the transceiver sizes can be optimized for different goals under some constraints. For systems with high performance requirements, the driver and receiver can be sized as to have minimum end-to-end delay. Similarly, for systems with constraints on energy, the driver/receiver sizes can be optimized for minimum total energy consumption.

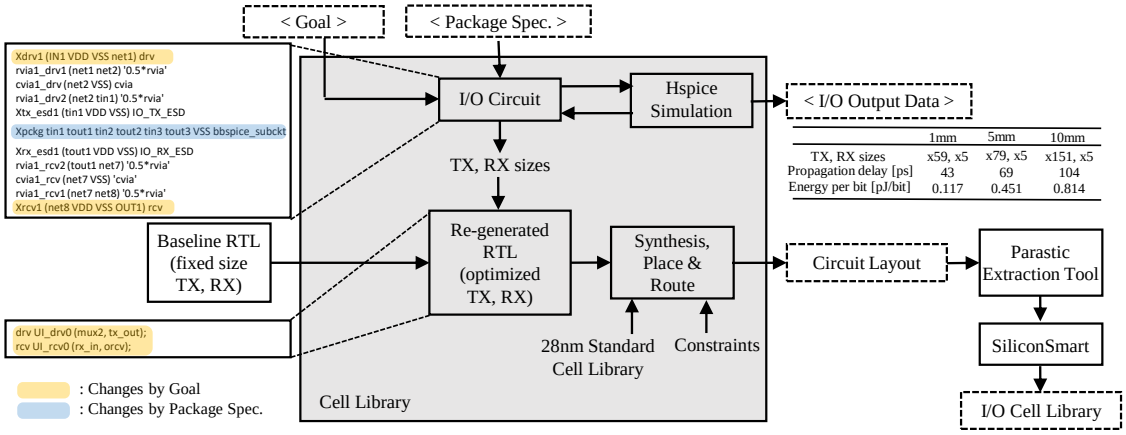

Figure 4.1: Proposed I/O cell library generation flow. A table and layout show an example of delay minimized I/O for 1mm interposer wire generated with the flow.

Figure. 4.1 shows the proposed I/O cell library generation flow. The transceiver circuits are considered as inverter chain. The sizes of the first and last inverter in the driver stage are defined as 1 and D, respectively. Likewise, the sizes of the first and last inverter stage in the receiver are defined as R and 1. Now, the design of the I/O cell can be defined as design of the entire driver and receiver chain, i.e. selecting final driver (D) and receiver (R) sizes, as well as number of inverters in the driver (N_{driver}) and receiver ($N_{receiver}$) chains. The tool flow consists of two main steps; I/O design specification and I/O library generation.

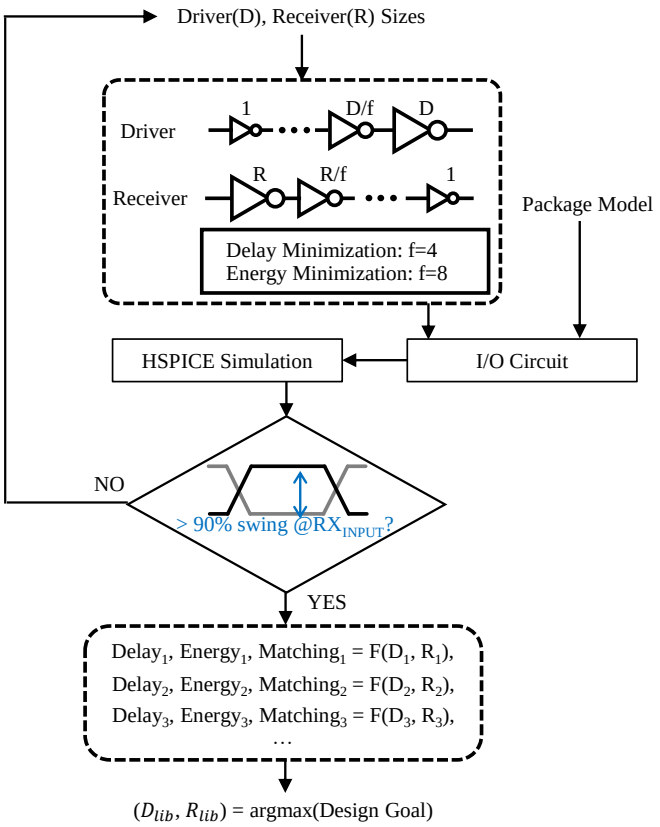

Figure 4.2: Methodology to I/O design specification.

4.1 I/O Design Specification

For each driver (D) and receiver (R) pair, an optimal ratio (f) between each stage of driver and receiver inverter chain is selected as shown in Figure. 4.2. Consider energy minimization as an example. For very large ratios (f), the number of stages required to drive a fixed final stage is small which reduces the switching power, but increases the short circuit power because slow slew rate dominates the total power. Similarly, for large number of stages (smaller f), the total power is dominated by switching power. Therefore, an optimal number of stages is selected for energy optimization with respect to ratio f and f=8 is obtained as optimum ratio. On the other hand, for propagation delay minimization, the driver and receiver chain is sized based on effective fanout (C_{drv}/C_{invx1}) and is obtained to be 4.

The next step is to select the optimal driver/receiver for energy and delay minimization.

Consider the example of delay minimization for a target wire length and interposer technology. The overall flow starts with a set of available driver and receiver sizes (i.e. set of R, and D). For each pair in the set, the elaboration of the entire driver/receiver chain is first perform based on f=4. Next, for all the driver/receiver options, co-simulation is performed where the wire model incorporates interposer technology and length properties. The subset of the driver/receiver pairs is selected which interposer output swing is greater than 90% of the ful l-swing and finally, from this subset, the optimum I/O cell is selected for minimum delay. The same process can be performed for minimum energy as well by using f=8 for elaboration.

4.1.1 I/O Library Generation

Once the driver/receiver chains are finalized, the proposed flow generates the RTL for these driver/receiver. The modified RTL is automatically inserted into a baseline template consisting of rest of the functional logic for the I/O cell. Using standard cell library, the RTL is synthesized and placed and routed to generate the layout for the I/O cell. The final layout and extracted netlist can be passed to a cell library characterization tool, such as SiliconSmart to generate the final timing and power library of the I/O cell.

CHAPTER 5
EXPERIMENTAL RESULTS

In this section, the applications of the proposed design flow is demonstrated for generation of I/O cells under various conditions. Subsection A, B show generated I/Os for various interposer models or wire lengths. Subsection C presents design methodology of I/Os for a SiP with many dies and comparison between traditional I/Os and generated I/Os from proposed flow. Subsection D compares single-ended and differential receivers and suggests considering both receivers for a SiP with non-neighboring connections. Subsection E shows design methodology of I/Os for a heterogeneous signaling and subsection F presents how generated I/Os are changed for ESD protections. For all subsections, driver/receiver sizes are presented as I/O designs for both delay and energy minimization scenarios. Drivers/receivers are considered as inverter chains and those sizes are defined as final/first inverter sizes. Inverter size of n is n times wider than inverter size of 1, which is the minimum size of inverter that the considered CMOS technology allows. The results are based on 28nm CMOS technology for transceiver and 65nm BEOL technology for silicon interposer.

5.1 Cell Library for Different Interposer

The interposer wire parasitics are dependent on wire dimensions as well as spacing/ shielding between wires. A higher wiring density is required for large bandwidth SiP systems. However, it leads to finer wire pitch and therefore higher resistive wires and more coupling capacitance. This limits the achievable data rates which in turn reduces the system bandwidth. To understand the role of transceiver optimization and to demonstrate the feasibility of the proposed flow for varying package wire dimensions, three cases of package wire dimensions are considered, as described in Figure. 5.1 and Table 5.1. 65nm BEOL tech-

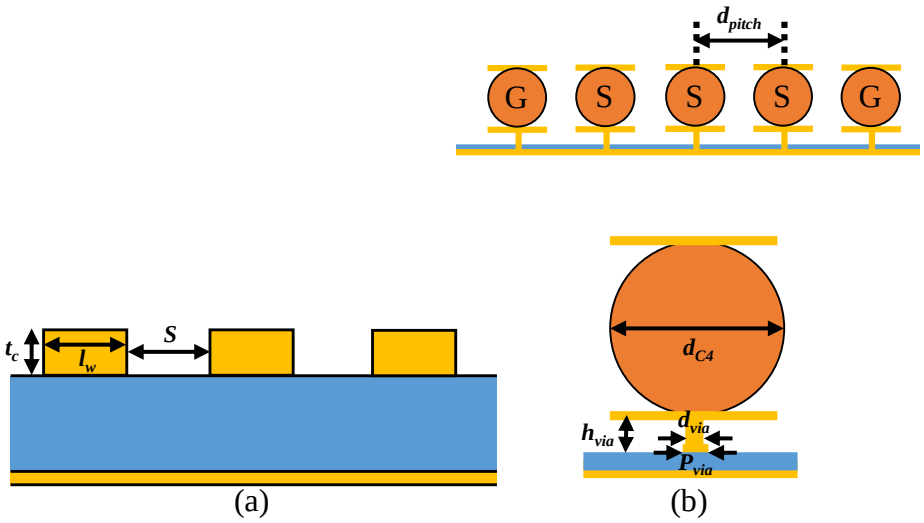

Figure 5.1: (a) Transmission line [28], (b) micro bump.

Table 5.1: Physical Dimensions of Various Package Models.

	Case1	Case2	Case3
Line Width(l_w)	0.4	1.6	1.6
Spacing(S)	0.4	1.6	1.6
Thickness(t_c) [μm]	1	2.0	2.0
Bump Diameter(d_{bump})	25	25	15
Pitch(d_{pitch}) [μm]	50	50	30
Chip to interposer Via Diameter(d_{via})	0.4	1.6	1.6
Pad(P_{via})	0.7	2.4	2.4
Height(h_{via}) [μm]	5.0	2.0	2.0

nology is assumed to determine the sample space for the interconnect geometry. Case 1 has minimum achievable line dimensions that provide the highest interconnect density and represents a high bandwidth SiP system. Case 2 has lower wiring density and represents a SiP system which can achieve higher data rates. Case 3 has reduced bump size/pitch with respect to other two cases to reduce wire lengths.

The generated delay and energy optimized I/O cells for these interposers in 1mm wire are shown in Table 5.2. The case 1 has smaller wire dimension than the case 2 and hence, requires stronger I/O driver (i.e. larger I/O cell) to drive more resistive wires. Likewise, the case3 has smaller bump dimensions than the case 2, which contribute significant parasitics

Table 5.2: I/O Cells for Various Interposer Models (1mm Wire).

	Delay Minimization			Energy Minimization		
	Case1	Case2	Case3	Case1	Case2	Case3
TX sizes	x72	x59	x80	x3	x3	x3
RX sizes	x5	x4	x5	x3	x1	x1
Propagation delay[ps]	45	43	43	193	164	193
Energy per bit[pJ/bit]	0.144	0.117	0.145	0.093	0.084	0.088

to the interposer channel and require larger I/O. As case 1 and 3 are more resistive than case 2, they require bigger driver/receiver sizes than case 2 for delay minimization. On the other hand, driver/receiver sizes for minimum energy are nearly same because x3 driver is the smallest size that achieves 90% voltage swing constraints for all interposer cases. Delay from the energy minimized I/O is much larger for case 1 and 3, compared to the one for case 2.

5.2 Cell Library for Different Wire Lengths

For large-scale integration of dies in a SiP, the D2D communication will cover a wide range of wire lengths. It is essential to design I/O circuit optimized for different ranges of wire lengths to achieve high data rates as well as to minimize energy consumption. The application of the proposed flow is presented for generating I/O cell for delay or energy minimization for different wire length.

Table 5.3: I/O Cells for Various Wire Lengths (Package Case2)

	Delay Minimization			Energy Minimization		
	1mm	5mm	10mm	1mm	5mm	10mm
TX sizes	x59	x79	x151	x3	x12	x28
RX sizes	x4	x5	x5	x1	x1	x3
Propagation delay [ps]	43	69	104	164	192	162
Energy per bit [pJ/bit]	0.117	0.451	0.814	0.0.084	0.337	0.639

Table 5.3 shows driver/receiver sizes, delay, energy for various lengths for delay or

energy minimization considering the interposer technology from case 2 in Figure. 5.1. In general, driver size increases with increasing wire lengths for both energy or delay minimization. Moreover, as expected, driver/receiver sizes, are bigger for delay minimization and smaller for energy minimization.

5.3 Case Study on An Illustrative SiP

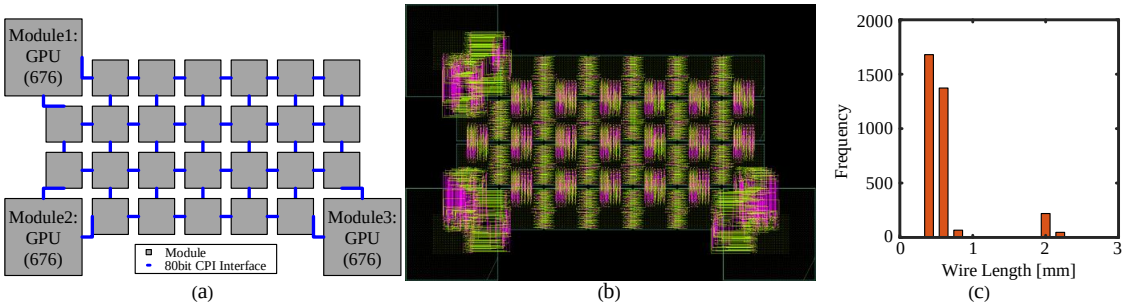

Figure 5.2: (a) Floor plan, (b) interposer routing layout, and (c) wire length distribution of a mesh NOC structure.

To demonstrate the feasibility of the proposed flow for a large-scale system, the proposed flow is applied to an illustrative SiP design as shown in Figure. 5.2(a). It consists of CPU, GPU, baseband and several other modules in mesh structure. Layout of interposer routing for the SiP system is separately generated and different colors present different metal layers (Figure. 5.2(b)). In this design, two metal layers are used on top of the interposer for the routing. The wire length distribution shows histogram of the interconnections in an interposer layer (Figure. 5.2(c)) and it has small range of wire lengths as it does not contain non-neighboring connections.

Traditionally, off-chip I/O cells are usually designed to match a target impedance ($\sim 50\Omega$) to minimize reflection in off-chip wires. Therefore, for a comparison, I/O cells are first designed to match target impedance. Table 5.4 (A) shows worst delay and average energy of these I/O cells, referred to as the conventional I/O cells. Table 5.4 (B, C) summarizes all the I/O cells that are created with the optimization methods discussed previously.

Table 5.4: I/O Cells for an Illustrative SIP (Interposer Case2)

	Conventional I/O (47Ω) (A)	Individual optimized I/O (B)		Optimized I/O for longest wire (C)	
		Delay Min.	Energy Min.	Delay Min.	Energy Min.
TX, RX sizes	x128, x4	x55-x82, x5	x2-x6, x1	x82, x5	x6, x1
Worst delay [ps]	55	51	167	51	167
Avg. energy [pJ/b]	0.187	0.089	0.060	0.099	0.063

I/O cells are optimized (delay or energy) individually for different wire-lengths (referred to as '*Individually optimized I/O*'). The worst-case delay and average energy (=total energy of all wires divided by the number of wires) are reported for analysis. Individually optimized I/Os for minimum delay, shows 13% less worst-case delay and 33% less average energy consumption compared to conventional I/O. Likewise, individually optimized I/Os for minimum energy, shows 198% higher worst-case delay but 52% less energy consumption compared to the conventional I/O. Table 5.4 (C) shows the result when only one I/O cell is generated using proposed flow considering delay or energy minimization for the maximum wire-length and placed for all length of wires. This design is referred as '*Optimized I/O for longest wire*'. Using the optimized I/O for longest wire for minimum delay results in 7% less worst-case delay and 36% less average energy consumption compared to the conventional I/O cell. Likewise, when optimized I/O to minimize energy dissipation for longest wire is used, 174% higher worst-case delay but 66% less average energy are observed. In summary, I/O cells are generated by proposed flow with lower worst-case delay as well as reduce average energy dissipation compared to conventional I/O.

5.4 Structure of Receivers

Single-ended receiver design is only considered for I/Os and adjust driver/receiver sizes for minimum delay and energy. A single-ended receiver has small area and energy, but vulnerable to noise and PVT variations. On the other hand, differential receiver is robust to noise and PVT variations, but has larger area and energy consumption. Differential

receiver is added in the I/O generation flow and the proposed tool can select single-ended or differential receivers (Figure. 5.3). Single-ended receiver is a chain of inverters and thus requires full-swing signal as input. In contrast, differential receiver can have low-swing signal as input. 90% voltage swing is set as constraint at receiver input for single-ended receiver, and 40% for differential receiver. These constraints cause different tendency of two receivers in propagation delay, energy, and area. In this subsection, the proposed flow is applied to analyze the propagation delay, energy, area, and reach (i.e. maximum wire length supported) of I/O circuits with single-ended drivers but single-ended or differential receivers. Given a wire length distribution, the flow suggests a methodology to choose the optimal receiver design for each I/Os depending on wire lengths in a SiP design.

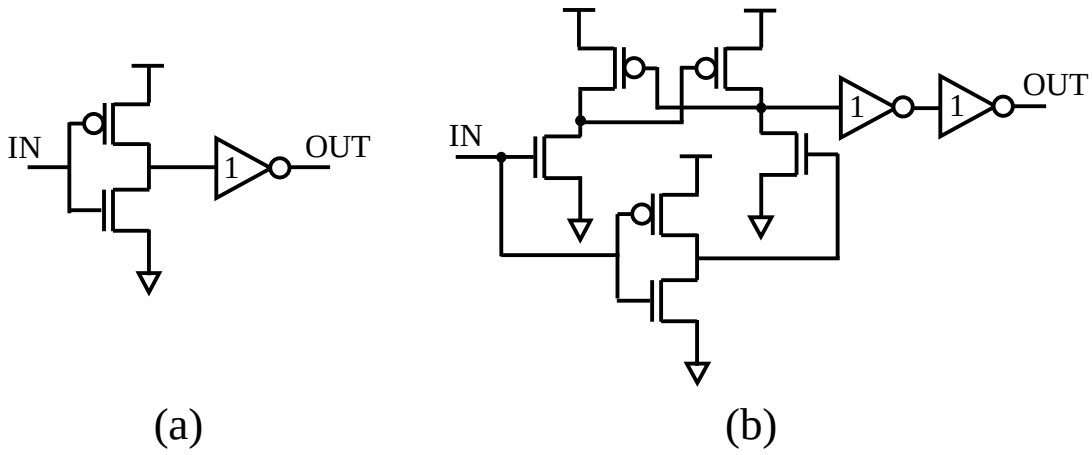

Figure 5.3: (a) Single-ended and (b) differential receiver circuits.

I/Os with fixed driver sizes

Firstly, a design is considered where the size of the driver is fixed for all I/O cells in an SiP. It will save design cost and effort for a large design. However, a fixed size driver can only drive single-ended signal through a maximum wire length, as voltage swing of the signal at the input of the receiver reduces as wires get longer. The I/O circuits with differential receivers can correctly detect input signals with much lower voltage swing than the I/Os with single-ended receivers. Hence, for a given size of driver, the I/O circuits

with differential receivers can drive much longer wires than the I/Os with single-ended receiver (Figure. 5.4). Maximum wire length of both single-ended and differential receiver changes by package property. Case1 package is more resistive than case2, so for a given driver size, the maximum drivable wire length for case1 interposer is smaller than the same for the interposer case2. Delay and energy of I/O with single-ended/differential receiver for given driver size/wire length is nearly same. (0-4.8%, 4-7.5% difference respectively) (Table. 5.5). Therefore, I/Os with single-ended receiver can be adopted for shorter wires (up to a maximum wire length), and differential receiver for longer wires.

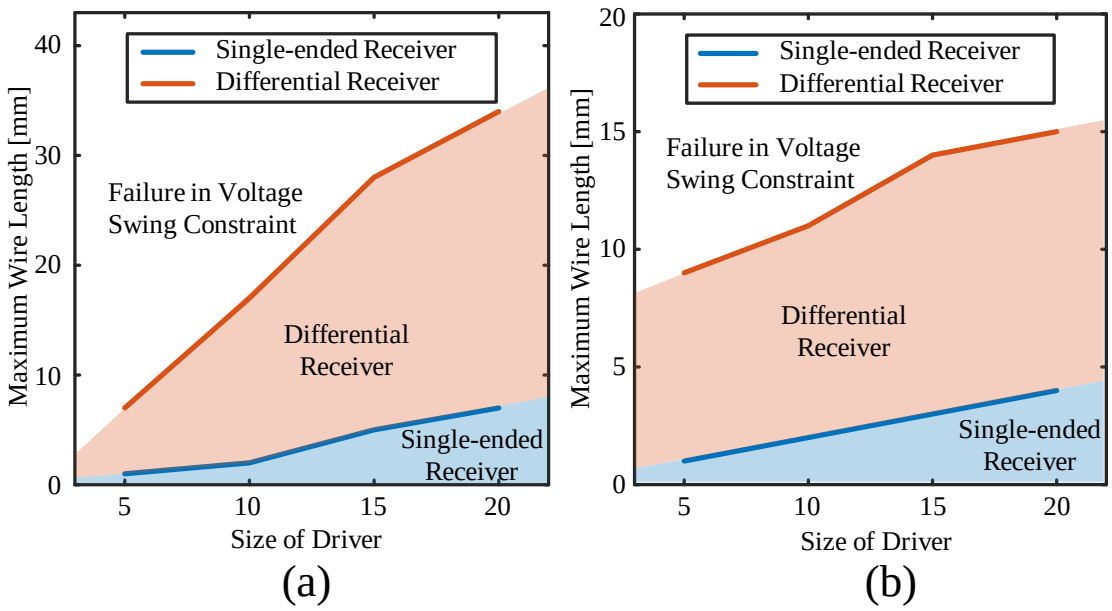

Figure 5.4: Maximum wire length that single-ended and differential receiver can drive on (a) case2 and (b) case1 interposer.

Figure. 5.5(a) shows a chipletized design of a generic SoC including CPU and GPU. Layout of interposer routing for the SiP system is seperately generated and different colors present different metal layers (Figure. 5.5(b)). In this design, three metal layers are used on top of the interposer for the routing. The wire length distribution shows histogram of the interconnections in an interposer layer (Figure. 5.5(c)). As this design contains non-neighboring connections, it has a large range of wire lengths (∼6mm) compared to Figure. 5.2(a), so single-ended receiver solely results strong driver that has large energy

Table 5.5: Delay/Energy/Area of I/O with Single-Ended/Differential Receiver for Given Driver Sizes.

	Delay [ps]		Energy [pJ/bit]		Area [μm^2]	
	Single-ended	Differential	Single-ended	Differential	Single-ended	Differential
x5	123	129	0.089	0.093	2.268	4.002
x10	84	84	0.088	0.093	2.898	4.632
x15	71	71	0.096	0.101	4.914	6.648
x20	64	61	0.095	0.103	5.418	7.152

and area. Maximum wire length of differential receiver with x5 driver (7mm) is longer than longest length of the distribution(6mm), so x5 driver can be used for all wire lengths. Maximum wire length of single-ended receiver with x5 driver is 1mm, so single-ended receiver is used for 1mm wire and differential receiver is used for 2-6mm. This set of I/Os has 306ps worst delay, 0.115pJ/bit average energy consumption, and 22.3μm^2 area.

Table 5.6: I/O Cells with All Single-Ended, All Differential, and Mix of Single-Ended and Differential Receiver for a Wire Length Distribution

	All Single-ended	All Differential	Single-ended & Differential
Driver sizes	x3 - x16	x2 - x5	x3 - x5
Worst delay [ps]	**189**	315	315
Average energy [pJ/bit]	0.170	**0.107**	0.152
Area [μm^2]	18.1	21.9	**18.0**

Energy minimized I/Os

I/O for a given wire is proportional to the size of driver, so minimum size of driver that satisfies the voltage swing constraint at receiver input may achieve both energy and area minimization. Fig. 5.6 (a), (b) shows the area of single-ended or differential receivers with minimum drivers for each length of wires. When the wire is short, I/O with single-ended receiver is smaller than I/O with differential receiver. This is because area of a differential

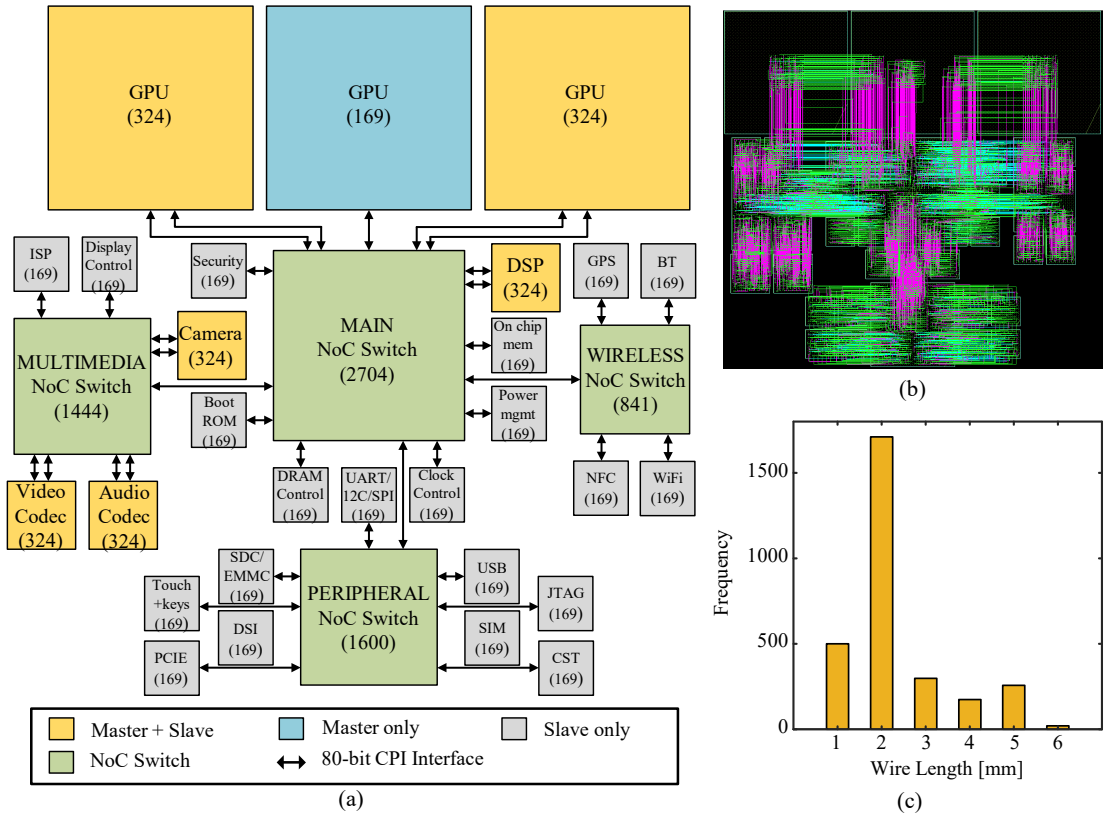

Figure 5.5: (a) Floor plan, (b) interposer routing layout, (c) wire length distribution of a chipletized generic SoC.

receiver (dark red) is bigger than the area of a single-ended receiver (dark blue). However, as wire becomes longer, the size of driver for single-ended receiver (light blue) grows faster than for differential receiver (light red) because of larger voltage swing constraint. Therefore, I/O with single-ended receiver occupies larger area than I/O with differential receiver for long wire. On the other hand, for all wire length, I/O with differential receiver has longer delay (25-105%) and less energy consumption (6-70%) compared to I/O with single-ended receiver (Fig. 5.6 (c),(d)). This is because I/O with differential receivers always have smaller driver size resulting in longer delay and smaller energy consumption.

The critical wire length after which I/O with single-ended receiver become larger than I/O with differential receiver varies by the interposer design. (Fig. 5.6 (a),(b)) Due to the higher wire resistance, the critical wire length for the interposer in case 1 is shorter than

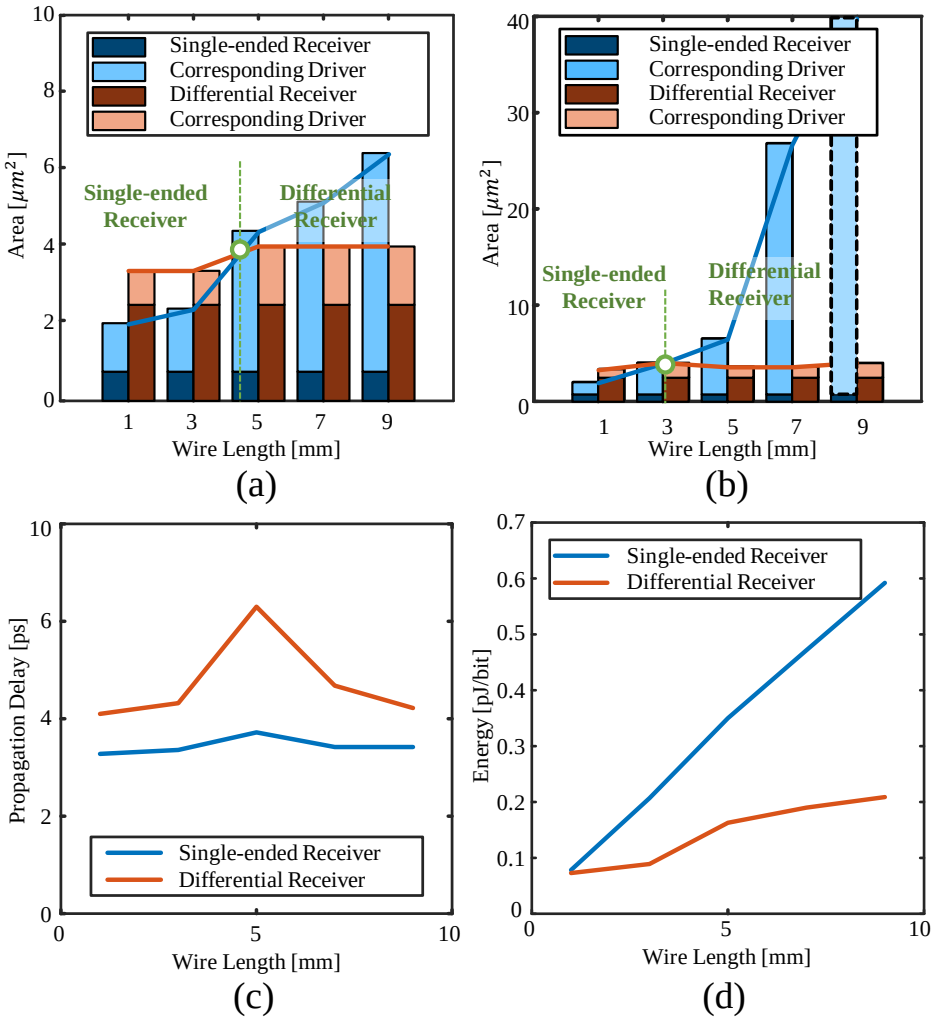

Figure 5.6: (a), (b) Area of driver and receiver for case2, case1 interposer respectively. (c) Propagation delay, (d) energy of I/O with single-ended and differential receiver for several wire lengths.

the same in case 2.

Consider the wire length distribution in Fig. 5.5 again. Given a wire length distribution, three approaches are considered to design energy-minimized I/O circuits: (Table. 5.6)

1. All I/Os with single-ended receivers and corresponding energy minimized driver. This set of I/Os decrease worst delay, because single-ended receiver always have smaller delay than differential.

2. All I/Os with differential receivers and corresponding energy minimized driver. In

this case, average energy is reduced because differential receiver always have smaller energy consumption.

3. A mix of I/Os with single-ended and I/Os with differential receivers, each with corresponding energy minimized drivers. I/Os can have single-ended receiver for a range of short wires and have differential receiver for longer wires, which leads to the area reduction.

In summary, worst delay, average energy, or area can be decreased by choosing single-ended or differential receiver for each length of wires.

5.5 Heterogeneous Signaling

The ability of heterogeneous signaling between different supply voltages or different technologies is one of the most important advantages in 2.5D SiP integration. I/O design for heterogeneous integration should also take into account supply voltages and technologies of two dies to achieve minimum delay or energy in the interconnect. Therefore, the automated I/O generation flow shows more benefit on heterogeneous integration. In this subsection, I/Os for signaling between two dies in 28nm and 180nm technologies with 0.9V and 1.8V supply voltages are presented respectively as an example. Figure. 5.7 shows two scenarios for heterogeneous signaling. Figure. 5.7(a) uses low voltage (0.9V) signaling from driver to interconnect and shift to high voltage (1.8V) at I/O 2 (180nm). Notice that differential receiver in Figure. 5.3 can also behave as level shifter, so additional level shifter is not required at slave. On the other hand, Figure. 5.7(b) uses high voltage (1.8V) signaling from driver to interconnect and shift to low voltage (0.9V) using differential receiver at I/O 1 (28nm). Other voltages than 0.9V or 1.8V do not considered for signaling since it requires level shifters at the input of driver in both I/Os and results larger delay and energy consumption.

Table. 5.7 presents worst delay and energy of delay/energy minimized I/Os for hetero-

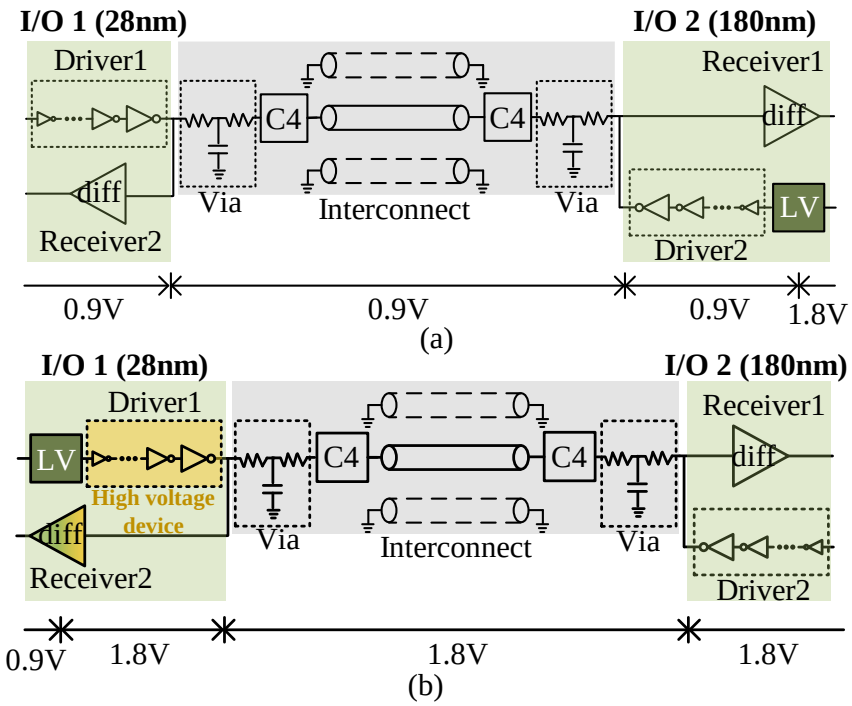

Figure 5.7: Two scenarios of heterogeneous signaling. (a) uses low voltage signaling and (b) uses high voltage signaling at interconnect.

geneous integration between 28nm and 180nm dies. Low voltage signaling in interconnect (Fig. 5.7(a)) results smaller worst energy consumption, but larger worst delay because driver2 (180nm) operates in low voltage (0.9V) when signal goes from 180nm to 28nm. On the other hand, high voltage signaling (Fig. 5.7(b)) arises larger worst energy, but smaller worst delay because driver1 (28nm) uses high voltage devices. Therefore, energy minimized I/O should use low voltage signaling and delay minimized I/O should use high

Table 5.7: I/O Cells for Heterogeneous Signaling between 28nm and 180nm Dies.

	Low V Signaling		High V Signaling	
	Delay min.	Energy min.	Delay min.	Energy min.
TX sizes (28nm)	x85	x11	x2 (HV)	x2 (HV)
TX sizes (180nm)	x38	x9	x38	x3
Worst delay [ps]	1023	1199	**977**	977
Worst energy [pJ/bit]	0.209	**0.157**	0.629	0.629

HV: high voltage device

voltage signaling in heterogeneous integration.

5.6 Cell Library with ESD protection

Transistor based ESD protection avoids a sudden electricity flow and protects integrated circuits. The delay/ energy minimized I/O cells with and without ESD protection are shown in Table 5.8. As ESD protection increases the load capacitance, I/O with ESD protection requires bigger driver/receiver sizes for delay minimization. On the other hand, driver/receiver sizes for minimum energy are same, but I/O with ESD protection consumes more energy.

Table 5.8: I/O Cells without and with ESD Protection (Interposer CASE2, 1mm)

	Delay Minimization		Energy Minimization	
	w/o ESD	w/ ESD	w/o ESD	w/ ESD
TX, RX sizes	x59, x4	x68, x5	x3, x1	x3, x1
Propagation delay [ps]	43	44	164	164
Energy per bit [pJ/bit]	0.117	0.125	0.084	0.087

CHAPTER 6
CONCLUSIONS

This paper presents automated flow for generating all-digital I/O library cells for large-scale 2.5D SiP integration. Given a 2.5D packaging (interposer) technology, the flow automatically generates I/O layout and timing/power library with the objective of minimizing delay or energy. It takes 7.9 min. to generate one delay/energy minimized I/O library for given interposer technology/wire length. The flow includes chip-interposer co-simulation to consider inductive property of on-interposer wire, and at the same time minimizes communication delay/energy, similar to buffer design/insertion for on-chip signaling. The proposed flow is demonstrated for various wire lengths, package dimensions, and ESD protections. Case studies of the flow is also presented on various SiP design to show its feasibility. The flow is first applied to generate I/O cells for an illustrative SiP design in mesh structure. Generated I/O cells show better delay/energy characteristics compared to traditional impedance matched I/O and dealy/energy minimizing design methodology of I/Os in large SiP design is suggested. The flow provides both single-ended and differential receivers options and the design methodology of I/Os is proposed for large SiP design with non-neighboring connections by using both receivers to meet the design goal. The flow also generates delay/energy minimized I/Os for heterogeneous signaling between 28nm and 180nm.

The interposer-based system-in-package integration is gaining traction in many industrial designs. There has been significant recent effort in developing standards for on-interposer signaling, for example, Intel's AIB [9]. The proposed flow can integrate with such emerging standard to enable automated I/O design for on-interposer wires. In addition, I/O cells generated from the proposed electronic design automation (EDA) flow can be easily integrated with the EDA flow for the full-chip design. For example, [29] has

adopted hard macro I/O cell generated from the flow and merged to the EDA flow for the full 2.5D IC design.

In the thesis, the experimental results are demonstrated based on delay or energy minimization as cost functions, motivated by on-chip signaling. Further considerations on cost functions beyond energy and/or delay minimization, such as impedance matching or area of I/O cells might be valuable in future work. Moreover, a co-design of I/O cells and interposer dimensions may provide more holistic design solution in SiP.

REFERENCES

[1] G. Gielen *et al.*, "Emerging Yield and Reliability Challenges in Nanometer CMOS Technologies," in *2008 Design, Automation and Test in Europe*, 2008, pp. 1322–1327.

[2] G. V. der Plas *et al.*, "Design Issues and Considerations for Low-Cost 3-D TSV IC Technology," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 293–307, 2011.

[3] K. Parat *et al.*, "A floating gate based 3D NAND technology with CMOS under array," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, pp. 3.3.1–3.3.4.

[4] T. Fukushima *et al.*, "New heterogeneous multi-chip module integration technology using self-assembly method," in *2008 IEEE International Electron Devices Meeting*, 2008, pp. 1–4.

[5] I. Bolsens, "Pushing the boundaries of Moore's Law to transition from FPGA to All Programmable Platform," in *Proceedings of the 2017 ACM on International Symposium on Physical Design*, ACM, 2017, pp. 23–23.

[6] J. Wang *et al.*, "High-speed and low-power 2.5D I/O circuits for memory-logic-integration by through-silicon interposer," in *2013 IEEE International 3D Systems Integration Conference (3DIC)*, 2013, pp. 1–4.

[7] K. Saban, "Xilinx Stacked Silicon Interconnect Technology Delivers Breakthrough FPGA Capacity , Bandwidth , and Power Efficiency," in *Xilinx, Tech. Rep. WP380*, 2011.

[8] E. McGill, "GLOBALFOUNDRIES Demonstrates 2.5D High-Bandwidth Memory Solution for Data Center, Networking, and Cloud Applications," *Global foundries*, 2017.

[9] D. Kehlet, "Accelerating innovation through a standard chiplet interface: the advanced interface bus (AIB)," *Intel Tech. WP-01285-1.1*, 2017.

[10] Daniel.S.Green, "Common Heterogenous Integration and Intellectual Property (IP) Reuse Strategies (CHIPS)," *CHIPS Proposers Day*, 2016, `https://www.darpa.mil/attachments/CHIPSoverview%20Sept212016ProposerDay.pdf`, last accessed on 2019-11-27.

[11] H. Zhang *et al.*, "Low-swing on-chip signaling techniques: effectiveness and robustness," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 8, no. 3, pp. 264–272, 2000.

[12] K. Chandrasekar *et al.*, "Timing analysis for wide IO memory interface applications with silicon interposer," in *2014 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2014, pp. 46–51.

[13] S. Lee *et al.*, "A 95fJ/b current-mode transceiver for 10mm on-chip interconnect," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 262–263.

[14] V. Raghunathan *et al.*, "A survey of techniques for energy efficient on-chip communication," in *Proceedings 2003. Design Automation Conference*, 2003, pp. 900–905.

[15] J. Bae *et al.*, "A 0.6pJ/b 3Gb/s/ch transceiver in 0.18 μm CMOS for 10mm on-chip interconnects," in *2008 IEEE International Symposium on Circuits and Systems*, 2008, pp. 2861–2864.

[16] R. Ho *et al.*, "High-Speed and Low-Energy Capacitively-Driven On-Chip Wires," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 2007, pp. 412–612.

[17] J. Seo *et al.*, "High-bandwidth and low-energy on-chip signaling with adaptive preemphasis in 90nm CMOS," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2010, pp. 182–183.

[18] D. Walter *et al.*, "A source-synchronous 90Gb/s capacitively driven serial on-chip link over 6mm in 65nm CMOS," in *2012 IEEE International Solid-State Circuits Conference*, 2012, pp. 180–182.

[19] B. Sawyer *et al.*, "Modeling, design, and demonstration of 2.5D glass interposers for 16-channel 28 Gbps signaling applications," in *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, 2015, pp. 2188–2192.

[20] V. Sundaram *et al.*, "Low-cost and low-loss 3D silicon interposer for high bandwidth logic-to-memory interconnections without TSV in the logic IC," in *2012 IEEE 62nd Electronic Components and Technology Conference*, 2012, pp. 292–297.

[21] S. Lee *et al.*, "Current-Mode Transceiver for Silicon Interposer Channel," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 9, pp. 2044–2053, 2014.

[22] W. S. Liao *et al.*, "3D IC heterogeneous integration of GPS RF receiver, baseband, and DRAM on CoWoS with system BIST solution," in *2013 Symposium on VLSI Circuits*, 2013, pp. C18–C19.

[23] M. Lin *et al.*, "An extra low-power 1Tbit/s bandwidth PLL/DLL-less eDRAM PHY using 0.3V low-swing IO for 2.5D CoWoS application," in *2013 Symposium on VLSI Technology*, 2013, pp. C16–C17.

[24] S. M. P. D. *et al.*, "A Q-Learning Based Self-Adaptive I/O Communication for 2.5D Integrated Many-Core Microprocessor and Memory," *IEEE Transactions on Computers*, vol. 65, no. 4, pp. 1185–1196, 2016.

[25] Y. Jeon *et al.*, "Design of an On-Silicon-Interposer Passive Equalizer for Next Generation High Bandwidth Memory With Data Rate Up To 8 Gb/s," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 7, pp. 2293–2303, 2018.

[26] D. Duvenaud *et al.*, "Additive Gaussian Processes," in *Proceedings of the 24th International Conference on Neural Information Processing Systems*, ser. NIPS'11, Granada, Spain, 2011, pp. 226–234, ISBN: 978-1-61839-599-3.

[27] H. M. Torun and M. Swaminathan, "High-Dimensional Global Optimization Method for High-Frequency Electronic Design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 6, pp. 2128–2142, 2019.

[28] H. M. Torun *et al.*, "A Bayesian Framework for Optimizing Interconnects in High-Speed Channels," in *2018 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO)*, 2018, pp. 1–4.

[29] J. Kim *et al.*, "Architecture, Chip, and Package Co-design Flow for 2.5D IC Design Enabling Heterogeneous IP Reuse," in *Proceedings of the 56th Annual Design Automation Conference 2019*, ser. DAC '19, Las Vegas, NV, USA, 2019, 178:1–178:6, ISBN: 978-1-4503-6725-7.